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| 10/577,057 | 04/24/2006 | Yohei Kanno | 740756-2956 | 9926 |

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| WARREN, MATTHEW E | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/577,057 | KANNO ET AL. | |
| | Examiner | Art Unit | |
| | MATTHEW E. WARREN | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 June 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-6 and 13-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 13-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4-24-06* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is in response to the Amendment filed on June 30, 2009.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wei et al. (US 5,156,986) in view of Mori et al. (US 5,243,202).

In re claim 1, Wei et al. shows (fig. ) a semiconductor element comprising: a layer comprising titanium (14) formed over a substrate (12); a gate electrode layer (16) formed over the layer comprising titanium; a gate insulating film (28) formed in contact with a top surface of the gate electrode layer and a top surface of the layer comprising titanium; a semiconductor film (30) formed over the gate insulating film; a pair of n-type impurity regions (32) formed over the semiconductor film; an insulating film (48) that is interposed between the pair of n-type impurity regions and that is formed over the semiconductor film; and a conductive layer (34, 36) formed over the pair of n-type impurity regions. Wei shows all of the elements of the claims except the insulating film having a laminated-layer structure. Mori shows (fig. 10) a semiconductor device comprising a gate electrode (112) formed on a substrate and a gate insulating film (120) formed on the gate electrode. The gate insulating film has a laminated structure of three

films (120a, 120b, and 120c) to provide an insulating film structure having a total breakdown voltage that is sufficiently high (col. 18, lines 25-43). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the gate insulating layer of Wei by forming a laminated-layer structure as taught by Mori to form a gate insulating layer with a sufficiently high breakdown voltage.

In re claim 2, Wei et al. shows (fig. ) a semiconductor element comprising: a layer comprising titanium (14) formed over a substrate (12); a gate electrode layer (16) formed over the layer comprising titanium; a gate insulating film (28) formed in contact with a top surface of the gate electrode layer and a top surface of the layer comprising titanium; a semiconductor film (30) formed over the gate insulating film; a pair of n-type impurity regions (32) formed over the semiconductor film; an insulating film (48) having a thickness of 100 nm (col. 8, lines 37-46) or more (2000 Å = 200 nm > 100 nm) that is interposed between the pair of n-type impurity regions and that is formed over the semiconductor film; and a conductive layer (34, 36) formed over the pair of n-type impurity regions. Wei shows all of the elements of the claims except the insulating film having a laminated-layer structure. Mori shows (fig. 10) a semiconductor device comprising a gate electrode (112) formed on a substrate and a gate insulating film (120) formed on the gate electrode. The gate insulating film has a laminated structure of three films (120a, 120b, and 120c) to provide an insulating film structure having a total breakdown voltage that is sufficiently high (col. 18, lines 25-43). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made

to modify the gate insulating layer of Wei by forming a laminated-layer structure as taught by Mori to form a gate insulating layer with a sufficiently high breakdown voltage.

In re claim 3, Wei et al. shows (fig. ) a semiconductor element comprising: a layer comprising titanium (14) formed over a substrate (12); a gate electrode layer (16) formed over the layer comprising titanium; a gate insulating film (28) formed in contact with a top surface of the gate electrode layer and a top surface of the layer comprising titanium; a semiconductor film (30) formed over the gate insulating film; a pair of n-type impurity regions (32) formed over the semiconductor film; an insulating film (48) that is interposed between the pair of n-type impurity regions and that is formed over the semiconductor film; and a conductive layer (34, 36) formed over the pair of n-type impurity regions, wherein a thickness of a portion of the semiconductor film over which the insulating layer is formed is thinner than that of the other portion of the semiconductor film (see fig. 14 or col. 8, lines 5-10), wherein the portion of the semiconductor film has a thickness of 10 nm or more (col. 7, lines 3-11) (2000 Å = 200 nm > 10 nm). Wei shows all of the elements of the claims except the insulating film having a laminated-layer structure. Mori shows (fig. 10) a semiconductor device comprising a gate electrode (112) formed on a substrate and a gate insulating film (120) formed on the gate electrode. The gate insulating film has a laminated structure of three films (120a, 120b, and 120c) to provide an insulating film structure having a total breakdown voltage that is sufficiently high (col. 18, lines 25-43). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made

to modify the gate insulating layer of Wei by forming a laminated-layer structure as taught by Mori to form a gate insulating layer with a sufficiently high breakdown voltage.

In re claim 4, Wei discloses (col. 8, line 37-46) that the insulating film comprises one of the materials of the group listed in the claims which is polyimide.

In re claim 6, Wei discloses (col. 1, lines 40-49) wherein the semiconductor element is incorporated in at least one selected from the group consisting of a TV reception set, an electronic book and a cellular phone (since the TFTs of the invention are employed in an LCD display which is used in a TV, electronic book, or cell phone).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable Wei et al. (US 5,156,986) in view of Mori et al. (US 5,243,202) as applied to claims 1-3 above and further in view of Sasaki et al (US 6,956,236).

In re claim 5, Wei and Mori disclose all of the limitations of the claims except the layer comprising titanium oxide. However Sasaki discloses wherein the layer comprises titanium oxide (40b Fig 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the layer with the specified material, since it has been held to be with the general sill of a worker in the art to select a known

material on the basis of its suitability for the intended use as a matter of obvious design choice. [In re Leshin, 125 USPQ 416].

Claims 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wei et al. (US 5,156,986) in view of Mori et al. (US 5,243,202) and Sasaki et al (US 6,956,236).

In re claim 13, Wei et al. shows (fig. ) a semiconductor element comprising: a layer comprising titanium (14) formed over a substrate (12); a gate electrode layer (16) formed over the layer comprising titanium; a gate insulating film (28) formed in contact with a top surface of the gate electrode layer and a top surface of the layer comprising titanium; a semiconductor film (30) formed over the gate insulating film; a pair of n-type impurity regions (32) formed over the semiconductor film; an insulating film (48) that is interposed between the pair of n-type impurity regions and that is formed over the semiconductor film; and a conductive layer (34, 36) formed over the pair of n-type impurity regions. Wei shows all of the elements of the claims except the insulating film having a laminated-layer structure. Mori shows (fig. 10) a semiconductor device comprising a gate electrode (112) formed on a substrate and a gate insulating film (120) formed on the gate electrode. The gate insulating film has a laminated structure of three films (120a, 120b, and 120c) to provide an insulating film structure having a total breakdown voltage that is sufficiently high (col. 18, lines 25-43). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made

to modify the gate insulating layer of Wei by forming a laminated-layer structure as taught by Mori to form a gate insulating layer with a sufficiently high breakdown voltage.

Wei discloses that the TFT is used in an LCD or imager (col. 1, lines 40-49) but does not disclose the complete invention comprising the pixel electrode. Wei and Mori disclose all of the elements of the claims except the pixel electrode electrically connected to the conductive layers. Sasaki et al. shows (fig. 1) an LCD having a pixel electrode (35) connected to conductive layers (48) of a TFT to form the LCD device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the TFT of Wei and Mori by electrically connecting a pixel electrode to the conductive layers of the TFT as taught by Sasaki to complete the LCD device.

In re claim 14, Wei et al. shows (fig. ) a semiconductor element comprising: a layer comprising titanium (14) formed over a substrate (12); a gate electrode layer (16) formed over the layer comprising titanium; a gate insulating film (28) formed in contact with a top surface of the gate electrode layer and a top surface of the layer comprising titanium; a semiconductor film (30) formed over the gate insulating film; a pair of n-type impurity regions (32) formed over the semiconductor film; an insulating film (48) having a thickness of 100 nm (col. 8, lines 37-46) or more (2000 Å = 200 nm > 100 nm) that is interposed between the pair of n-type impurity regions and that is formed over the semiconductor film; and a conductive layer (34, 36) formed over the pair of n-type impurity regions. Wei shows all of the elements of the claims except the insulating film

having a laminated-layer structure. Mori shows (fig. 10) a semiconductor device comprising a gate electrode (112) formed on a substrate and a gate insulating film (120) formed on the gate electrode. The gate insulating film has a laminated structure of three films (120a, 120b, and 120c) to provide an insulating film structure having a total breakdown voltage that is sufficiently high (col. 18, lines 25-43). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the gate insulating layer of Wei by forming a laminated-layer structure as taught by Mori to form a gate insulating layer with a sufficiently high breakdown voltage.

Wei discloses that the TFT is used in an LCD or imager (col. 1, lines 40-49) but does not disclose the complete invention comprising the pixel electrode. Wei and Mori disclose all of the elements of the claims except the pixel electrode electrically connected to the conductive layers. Sasaki et al. shows (fig. 1) an LCD having a pixel electrode (35) connected to conductive layers (48) of a TFT to form the LCD device. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the TFT of Wei and Mori by electrically connecting a pixel electrode to the conductive layers of the TFT as taught by Sasaki to complete the LCD device.

In re claim 15, Wei et al. shows (fig. ) a semiconductor element comprising: a layer comprising titanium (14) formed over a substrate (12); a gate electrode layer (16) formed over the layer comprising titanium; a gate insulating film (28) formed in contact with a top surface of the gate electrode layer and a top surface of the layer comprising

titanium; a semiconductor film (30) formed over the gate insulating film; a pair of n-type impurity regions (32) formed over the semiconductor film; an insulating film (48) that is interposed between the pair of n-type impurity regions and that is formed over the semiconductor film; and a conductive layer (34, 36) formed over the pair of n-type impurity regions, wherein a thickness of a portion of the semiconductor film over which the insulating layer is formed is thinner than that of the other portion of the semiconductor film (see fig. 14 or col. 8, lines 5-10), wherein the portion of the semiconductor film has a thickness of 10 nm or more (col. 7, lines 3-11) (2000 Å = 200 nm > 10 nm). Wei shows all of the elements of the claims except the insulating film having a laminated-layer structure. Mori shows (fig. 10) a semiconductor device comprising a gate electrode (112) formed on a substrate and a gate insulating film (120) formed on the gate electrode. The gate insulating film has a laminated structure of three films (120a, 120b, and 120c) to provide an insulating film structure having a total breakdown voltage that is sufficiently high (col. 18, lines 25-43). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the gate insulating layer of Wei by forming a laminated-layer structure as taught by Mori to form a gate insulating layer with a sufficiently high breakdown voltage.

Wei discloses that the TFT is used in an LCD or imager (col. 1, lines 40-49) but does not disclose the complete invention comprising the pixel electrode. Wei and Mori disclose all of the elements of the claims except the pixel electrode electrically connected to the conductive layers. Sasaki et al. shows (fig. 1) an LCD having a pixel electrode (35) connected to conductive layers (48) of a TFT to form the LCD device.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the TFT of Wei and Mori by electrically connecting a pixel electrode to the conductive layers of the TFT as taught by Sasaki to complete the LCD device.

In re claim 16, Wei discloses (col. 8, line 37-46) that the insulating film comprises one of the materials of the group listed in the claims which is polyimide.

In re claim 17, Wei discloses all of the limitations of the claims except the layer comprising titanium oxide. However Sasaki discloses wherein the layer comprises titanium oxide (40b Fig 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the layer with the specified material, since it has been held to be with the general sill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. [In re Leshin, 125 USPQ 416].

In re claim 18, Wei discloses (col. 1, lines 40-49) wherein the semiconductor element is incorporated in at least one selected from the group consisting of a TV reception set, an electronic book and a cellular phone (since the TFTs of the invention are employed in an LCD display which is used in a TV, electronic book, or cell phone).

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-6 and 13-18 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW E. WARREN whose telephone number is (571)272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matthew E Warren/
Primary Examiner, Art Unit 2815